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GB 2220315 A GB 2105130 A GB 2063020 A
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(54) **AM demodulator for I/Q receivers**

(57) I and Q outputs of a conventional I/Q receiver are full wave rectified and applied to a computing device which has an output equal to the square root of the sum of the squares of its two inputs. When the receiver input signal is an amplitude modulated carrier and the receiver local oscillator is close to the frequency of the incoming carrier then an output proportional to the amplitude of the modulation will be generated. The computing device may be an analogue circuit (fig. 2, not shown) or a digital computer. The receiver operates a synchronously due to the slight difference between received carrier and local oscillator frequencies.

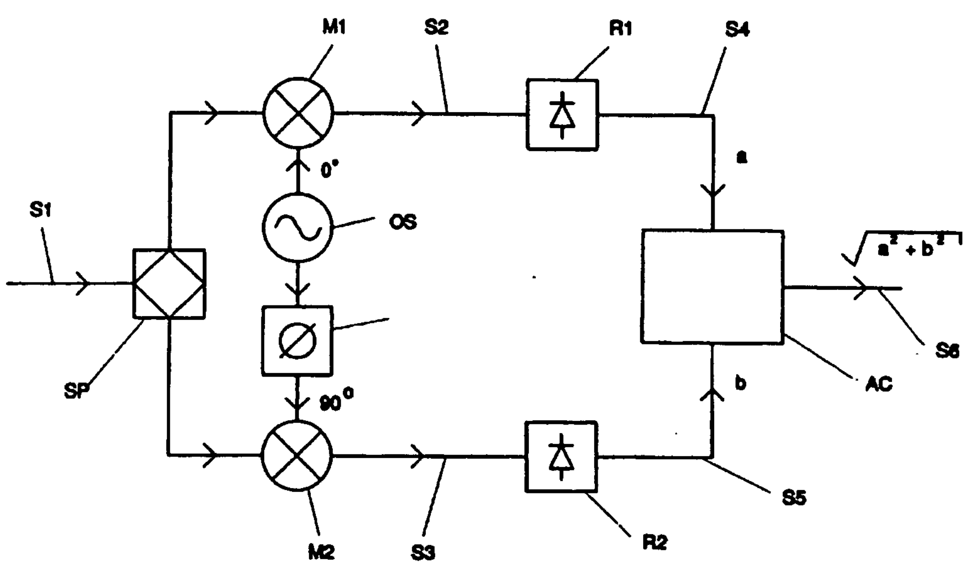

Fig.1

The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1995

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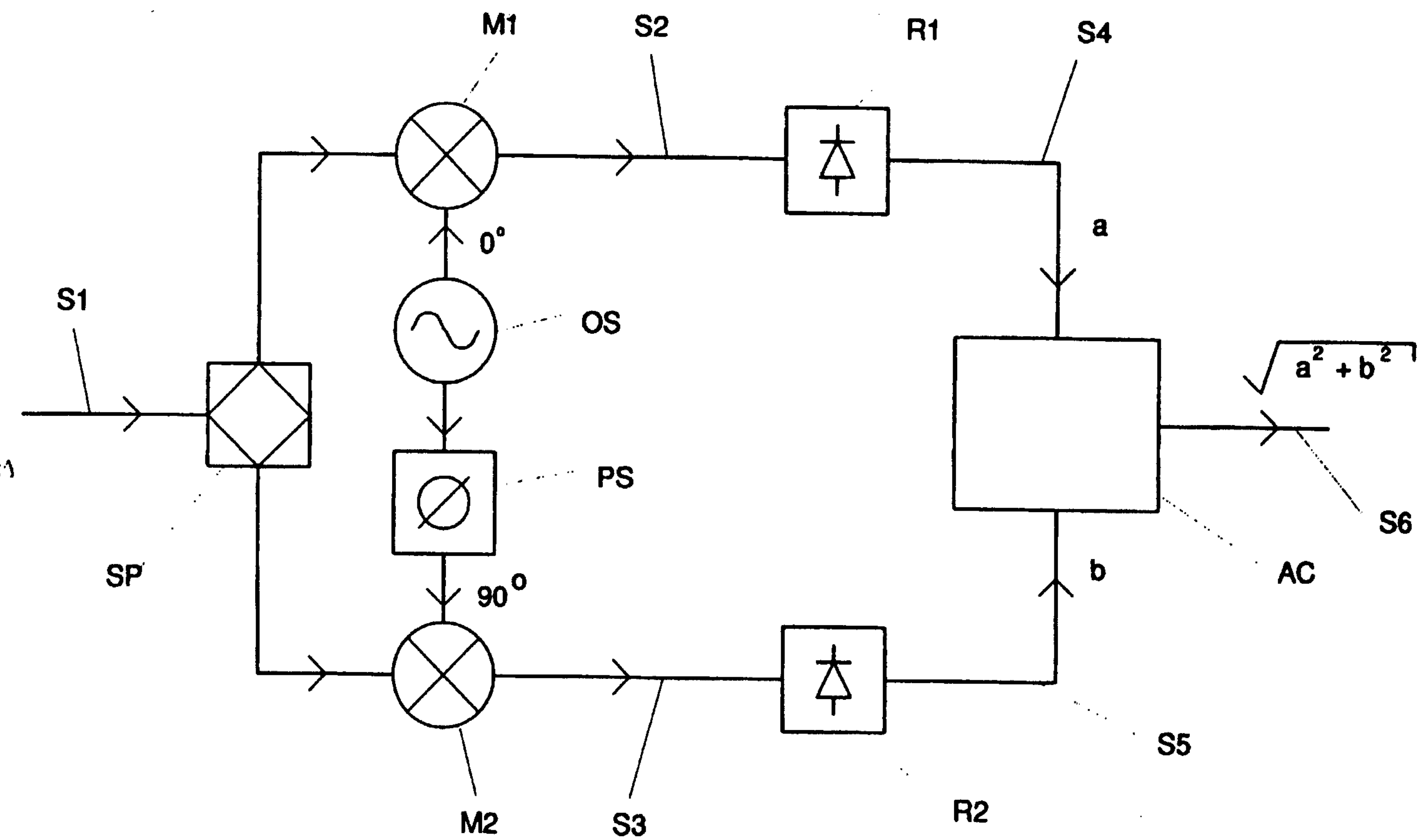

Fig.1

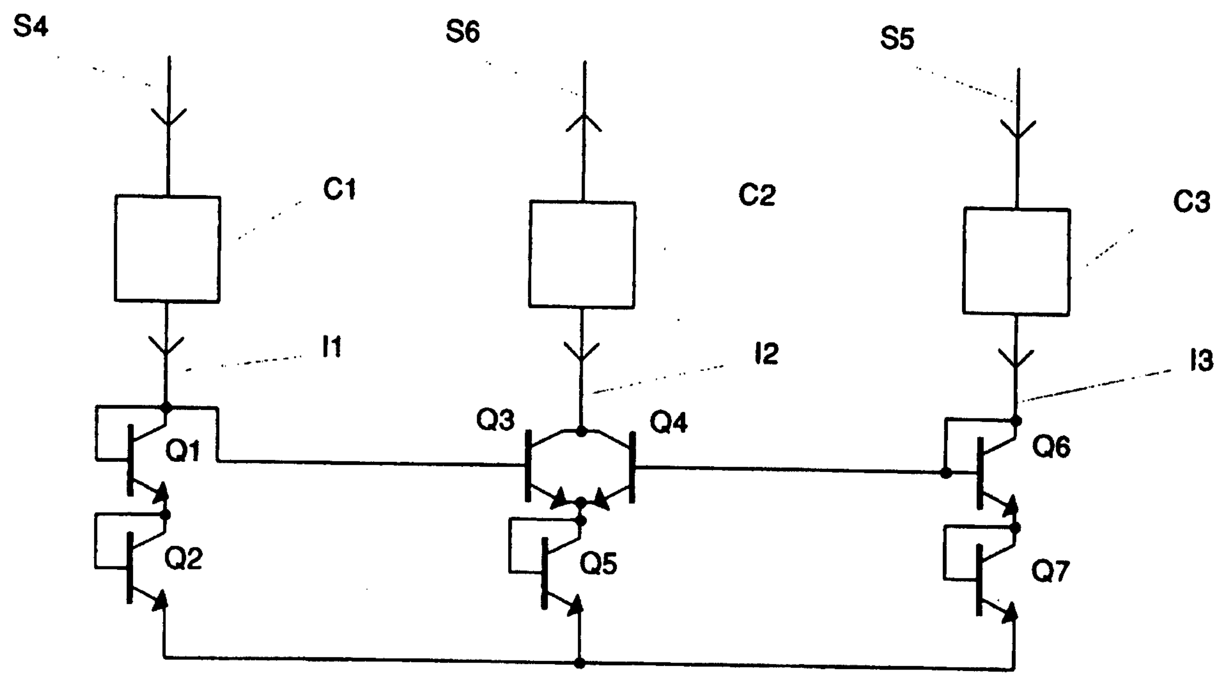

Fig.2

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AM Demodulator for I/Q Receivers

Radio receivers for amplitude modulated signals generally use the superheterodyne principle before applying a fixed intermediate frequency signal to a rectifier circuit. The trend now is to use, where possible, the zero intermediate frequency or direct conversion principle. These are usually described as I/Q receivers. I/Q techniques are also used in receivers designed to receive digitally encoded transmissions but amplitude detection may also be required to control the gain of amplifier stages within the receiver in a feedback loop.

Accurate amplitude sensing requires a different approach in I/Q receivers. One approach is to use synchronous demodulation with a phase locked local oscillator.

This invention relates to a simple method of asynchronously demodulating am signals in an I/Q type of receiver thus eliminating the complexity of phase locked synchronous receivers. This produces the direct conversion equivalent of the superheterodyne receiver with diode detector when used for the reception of am sound broadcasts for example.

Compared with superheterodyne receivers, direct conversion receivers offer the advantages of greatly reduced susceptibility to spurious reception on

unwanted channels, easier bandwidth control using active or passive audio filters so eliminating IF wound transformers and/or expensive ceramic ladder filters conventionally employed. The number of oscillators is also reduced to one.

Such an architecture lends itself very well to large scale integrated circuits for single chip am receiver applications,

According to the invention the I and Q outputs of a conventional I/Q receiver are full wave rectified and applied to a computing device which has an output equal to the square root of the sum of the squares of its two inputs. When the receiver input signal is an amplitude modulated carrier and the receiver local oscillator is within a certain proximity to the frequency of the incoming carrier then an output proportional to the amplitude of the modulation will be generated.

Figure 1. shows one embodiment of the invention. An am modulated signal is applied to the input, S1, of a splitter, SP. The two equal outputs of SP are applied to the mixers M1 and M2. Oscillator, OS, generates a signal whose frequency is close to that of the incoming signal. One output of the oscillator, OS, drives the mixer M1 whilst the other output is phase shifted 90 degrees by PS and applied to mixer M2. S2 and S3 represent the

outputs of mixers M1 and M2 respectively. The signal at S2 represents the I output and that at S3 the Q output as is well known. I refers to in-phase and Q to phase quadrature being the vector components of the carrier down converted to near zero frequency.

Bandpass filters and gain controlled amplifiers are normally present in paths S2 and S3 but are not shown for simplicity nor does their inclusion or absence materially alter the functioning of the invention,

The I/Q signals at S2 and S3 are rectified by full wave rectifiers R1 and R2 respectively. The outputs of the rectifiers a and b, at S4 and S5 are of equal magnitude and applied to the computing circuit AC. The computation of AC is such that S6 provides a signal corresponding to the square root of the sum of the squares of a and b.

Figure 2. shows an analogue embodiment of the computing device AC. C1 and C3 are voltage to current converters. C2 is a current to voltage converter. C1 and C2 derive their inputs from paths S4 and S5 and produce output currents I1 and I3 directly proportional to their input voltages at S4 and S5. Output current, I2, from the transistor array, Q1-Q7, produces a proportional output voltage from C2 at S6. Overall, the voltage at S6 is proportional to the amplitude of the input carrier signal at S1 of figure 1.

The transistor array, Q1-7, is one of a number of well known methods of making this computation. See, for example, Analogue IC Design: the Current Mode Approach, IEE, 1990, ch.2, B.Gilbert.

In practice dc coupled amplifiers may not be feasible in the I/Q paths and some allowance has to be made for the zero response at down conversion to frequencies below the low frequency cut off, say fc Hz, of ac coupled amplifiers. This corresponds to a need to maintain a working local oscillator frequency, incoming carrier frequency difference greater than +/-fc Hz. The upper limit on the allowable frequency error is determined by the bandwidth of the signal and the bandwidth of the filters in the receiver. Thus tuning of the receiver is generally necessarily asynchronous but otherwise duplicates conventional diode detection receiver operation. No whistles are produced when tuning in and the audio remains intelligible throughout.

The analogue signal processing can alternatively be carried out by digital computing methods to produce an equivalent result.

Claims

1. An I/Q receiver having firstly an in-phase output and secondly a quadrature output both full wave rectified and applied to a computing circuit which generates an output proportional to the square root of the sum of the squares of the two inputs thereof.

2. An I/Q receiver as claimed in claim 1 operable to receive a signal carrier wherein the receiver local oscillator frequency is close to the input carrier frequency and the computed output is proportional to the input carrier amplitude.

3. An I/Q receiver as claimed in claim 1 wherein the computing circuit includes a seven transistor array such that the inputs and outputs thereof are relative currents.

4. An I/Q receiver as claimed in claim 1 wherein the computing circuit is an analogue circuit.

5. An I/Q receiver as claimed in claim 1 wherein the computing circuit is mainly substituted by a digital computer performing the same computation.

6. An I/Q receiver as claimed in claim 1 operable to demodulate amplitude modulated input signals.

7. An I/Q receiver as claimed in claim 1 operable to detect input signal amplitude.

8. An I/Q receiver as claimed in claim 1 operable in an automatic gain control system.

9. An I/Q receiver as claimed in claim 1 wherein the I and Q outputs are AC coupled.

10. An I/Q receiver as claimed in claim 1 operable to receive and demodulate AM sound broadcast signals.

11. An I/Q receiver substantially as herein described with reference to figures 1 and 2.

The Patent Office

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Claims searched:	ALL	**Date of search:**	24 January 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H3R: RADA, RADB, RADC, RADD, RADX: H4P: PAQ

Int Cl (Ed.6): H03D, H04L

Other: Online: WPI, JAPIO, INSPEC, EDOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
Y	GB2220315 A	PHILIPS - see especially figures 1, 2 and lines 17-24 on page 3	5
X	GB2105130 A	UNITED - see especially the figure and lines 15-21 on page 2	1, 2, 4, 6, 7
X	GB2063020 A	PLESSEY - see especially figure 2 and lines 86-112 on page 2	1, 2, 4, 6, 7
Y			5
X	EP0099703 A2	FUJITSU - see especially figures 2, 3 and lines 26-34 on page 8	1, 2, 4, 6, 7

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.